REMARKS

This Amendment is responsive to the Office Action dated January 11, 2006. All rejections and objections of the Examiner are respectfully traversed. Reconsideration and further examination are respectfully requested.

At paragraphs 4 through 15 the Examiner rejected claims 1 through 8 and 10 as being obvious under 35 U.S.C. 103, citing United States patent number 6,625,654 of Wolrich et al. ("Wolrich et al."), in combination with United States patent number 6,965,615 of Kerr et al. ("Kerr et al."). Applicants respectfully traverse this rejection.

As noted in the previous response, Wolrich et al. discloses a parallel, hardware-based multithreaded processor, including a general purpose processor that coordinates system functions, and a plurality of microengines that support multiple program threads. The Wolrich et al. processor also includes a memory control system that has a first memory controller that sorts memory references based on whether the memory references are directed to an even bank or an odd bank of memory, and a second memory controller that optimizes memory references based upon whether the memory references are read references or write references. A program thread communication scheme for packet processing is also described in Wolrich et al.

Kerr et al. disclose a technique for striping packets across pipelines of a processing engine within a network switch. The processing engine of Kerr et al. includes multiple processors arrayed as pipeline rows and columns embedded between input and output buffers of the engine. Each pipeline row or cluster in the Kerr et al. system includes a context memory having a plurality of window buffers of a defined size. Each packet is apportioned into fixed-sized contexts corresponding to the defined window size associated with each buffer of the context

memory. The Kerr et al. technique includes a mapping mechanism for correlating each context with a relative position within the packet, i.e., the beginning, middle and end contexts of a packet. The mapping mechanism of Kerr et al. facilitates reassembly of the packet at the output buffer, while obviating any out-of-order issues involving the particular contexts of a packet.

Nowhere in the combination of Wolrich et al. and Kerr et al. is there disclosed or suggested any method or system for sharing at least one computer resource between a plurality of instruction threads of a multi-threaded process, including:

> providing a processor including a plurality of analysis machines and a plurality of computer resources, wherein each of said plurality of analysis machines includes an internal pipeline and is communicably coupled to a plurality of shared pipelines, wherein each said internal pipeline is an integer pipeline that starts the execution of every instruction that executes in said analysis machine in which it is included, ***wherein each said analysis machine includes pre-classification hardware, wherein said pre-classification hardware classifies a plurality of packet types while data is transferred by an instruction thread of said analysis machine into a packet header memory of said analysis machine for subsequent microcode access;***
>
> executing each instruction thread in one of the plurality of analysis machines; and
>
> sharing services of at least one of the plurality of computer resources between at least two of the plurality of analysis machines during the execution of each instruction thread (emphasis added)

as in the present independent claim 1. Analogous features are also present in the present independent claim 5. In contrast, Wolrich et al. teach only as follows with regard to classification, beginning at line 5 of column 2:

> The hardware-based multithreaded processor 12 also includes a central controller 20 that assists in loading microcode control for other resources of the hardware-based multithreaded processor 12 and performs other general purpose computer type functions such as handling protocols, exceptions, extra support for packet processing where the microengines pass the packets off for more detailed processing such as in boundary conditions . . .

Kerr et al. is similarly lacking, stating beginning at line 47 of column 5 as follows with regard to loading the context memory:

> The processors (TMC 0,1) of each cluster 345 execute operations on the transient data loaded into the context memory 500 by the input buffer 360, whereas the processors of each column operate in parallel to perform substantially the same operation on the transient data, but with a shifted phase. The processors of a cluster inherently implement first in, first out (FIFO) ordering primarily because there is no mechanism for bypassing processors within the cluster.

Thus Kerr et al. also includes no hint or suggestion of any kind of pre-classification hardware, as in the present independent claims 1 and 5.

For the above reasons, Applicants respectfully urge that the combination of Wolrich et al. and Kerr et al. does not disclose or suggest all the features of the present invention as set forth in independent claims 1 and 5. Accordingly, the combination of Wolrich et al. and Kerr et al. does not render the present independent claims 1 and 5 obvious under 35 U.S.C. 103. As to dependent claims 2-4, 6-8, and 10, they each depend from independent claims 1 and 5, and are respectfully believed to be patentable over the combination of Wolrich et al. and Kerr et al. for at least the same reasons.

At paragraphs 16-25 of the Office Action, the Examiner rejected claims 9 and 11-18 for obviousness under 35 U.S.C. 103, again citing Wolrich et al. and Kerr et al., and additionally citing United States patent number 6,081,860 of Bridges et al. ("Bridges et al."). Applicants respectfully traverse this rejection.

As noted in the previous response, Bridges et al. disclose a process and system in which master and slave devices are connected by a single address bus, a write data bus and a read data bus. The arbiter device of Bridges et al. receives requests for data transfers from the master

devices and selectively transmits the requests to the slave devices. The design of the Bridges et al. system is configured to advantageously function in mixed systems which may include address-pipelining and non-address-pipelining slave devices. The relevant teachings of Wolrich et al. and Kerr et al. are discussed above.

Nowhere in the combination of Wolrich et al., Kerr et al. and Bridges et al. is there disclosed or suggested any system for sharing at least one computer resource between a plurality of instruction threads of a multi-threaded process, including:

> a plurality of analysis machines to execute a plurality of instruction threads, wherein each of said plurality of analysis machines includes an internal pipeline and is communicably coupled to a plurality of shared pipelines, wherein each said internal pipeline is an integer pipeline that starts the execution of every instruction that executes in said analysis machine in which it is included, ***wherein each said analysis machine includes pre-classification hardware, wherein said pre-classification hardware classifies a plurality of packet types while data is transferred by an instruction thread of said analysis machine into a packet header memory of said analysis machine for subsequent microcode access;***
>
> a plurality of computer resources operationally connected to said plurality of analysis machines;
>
> wherein each instruction thread executes in one of said plurality of analysis machines, and services of at least one of said plurality of computer resources are shared between at least two of said plurality of analysis machines during the execution of each instruction thread. (emphasis added)

as in the present independent claim 5, from which dependent claims 9 and 11-18 depend. As noted above, Wolrich et al. teaches a system for parallel processing that is an alternative to a pipelined machine, and Kerr et al. describes a system for striping packets across pipelines. Bridges et al. describe a technique for enhancing a processor local bus to allow for address pipelining, but also provide no hint or suggestion of any method or system for providing pre-classification hardware in each of a plurality of analysis machines, wherein the pre-classification

hardware classifies a plurality of packet types while data is transferred by an instruction thread of each analysis machine into a packet header memory of the analysis machine for subsequent microcode access, as in the present independent claim 5. Thus the combination of Wolrich et al., Kerr et al. and Bridges et al. provides no teaching of significant features of the present independent claim 5.

For the above reasons, Applicants respectfully urge that the combination of Wolrich et al., Kerr et al. and Bridges et al. fails to disclose or suggest all the features of the present independent claim 5, from which claims 9 and 11-18 depend. Accordingly, the combination of Wolrich et al., Kerr et al. and Bridges et al. does not support a *prima facie* case of obviousness under 35 U.S.C. 103 with regard to the present independent claim 5, and dependent claims 9 and 11-18 are respectfully believed to be patentable over the cited combination for at least the same reasons. Reconsideration of all pending claims is respectfully requested.

For these reasons, and in view of the above amendments, Applicants respectfully request that all rejections and objections of the Examiner be withdrawn. The application is now considered to be in condition for allowance, and such action is earnestly solicited.

Applicants have made a diligent effort to place the application in condition for allowance. However, should there remain unresolved issues that require adverse action, it is respectfully requested that the Examiner telephone David A. Dagg, Applicants' Attorney at 617-630-1131 so that such issues may be resolved as expeditiously as possible.

Respectfully Submitted,

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Date

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